Curriculum Vitae

William C. Athas

Employment background

12/97 to present:	Senior Project Leader, Information Sciences Institute, University of Southern Calif., Marina del Rey, Calif.
04/95 to present:	Research Assistant Professor of EE-Systems, University of Southern Calif., Los Angeles, Calif.
08/91 to 12/97:	Project Leader, Information Sciences Institute, University of Southern Calif., Marina del Rey, Calif.
01/90 to 08/91:	Member of Research and Technology Staff, Northrop Research and Technology Center, Palos Verdes, Calif.
08/88 to 12/89:	Assistant Professor of Computer Science, The University of Texas at Austin, Austin, Texas.
07/87 to 08/88:	Research Fellow of Computer Science, The California Institute of Technology, Pasadena, Calif.
10/85 to 06/87:	Engineering Consultant, Symult Systems Corporation, Monrovia, Calif.

Educational background

Ph.D., California Institute of Technology, Computer Science, June 1987.

M.S., California Institute of Technology, Computer Science, June 1983.

B.S., The Univ. of Utah, Major/Minor: Computer Science/Physics, June 1981.

Major research contracts:

DARPA/ITO, "Architecture for Real-Time Decoupled Execution," January 2000 - December 2000, $171,501.

National Institute of Health, "Hearing Aid Research Project," August 1998 - July 2001, $668,246. Principal Investigator

MicroDisplay, Inc., "MD-1: Ultra Low-Power Microprocessor for the MicroDisplay LCD Prototype System," October 1997 - July 1998, $308,000. Project Leader.

DARPA/ITO, "Energy-Recovery CMOS for Ultra-Low-Power Applications," October 1995 - September 1998, $1,719,569. Project Leader

EXHIBIT 1
PAGE 8

DARPA/ITO, "Scalable Desktop HPC Software," October 1995 - September 1997, $660,780. Project Leader.

DARPA/ETO, "Pulsed-Power Techniques for Portable and Embedded Computing Systems," May 1996 - April 1999, $1,644,522. Project Leader.

DARPA/CSTO, "Embeddable High-Density Microsystems," October 1994 - November 1995, $1,231,564. Project Leader.

DARPA/ESTO, "Adiabatic Switching Circuits Project," September 1992 - August 1996, $1,275,963. Project Leader.

Patents

"A Mechanism for Power-Efficient, Pulsed Driving of Capacitive Loads to Controllable Voltage Levels," patent pending, 1999.

"Line-Reflection Cancellation with Energy-Recovery Driver," provisional patent filed, 1999.

"High-Performance Clock-Powered Logic," provisional patent filed, 1999.

"Highly Efficient, Complementary, Resonant Pulse Generation," first inventor. US Patent #5,559,478. Assigned to the University of Southern California, 1996.

"System and Method for Power-Efficient Charging and Discharging of a Capacitive Load from A Single Source," co-inventor. US Patent #5,473,526. Assigned to the University of Southern California, 1995.

"Asynchronous Circuit for 2-Cycle to 4-Cycle Handshake Conversion," sole inventor. US Patent #5,388,241. Assigned to Northrop Corp., 1992

"Apparatus for Intrasystem Communications within a Binary N-cube Including Buffer Lock Bit," first inventor. US Patent #5,047,917. Assigned to the California Institute of Technology, 1989.

"High Performance Dynamic RAM Interface," co-inventor. US Patent #4,937,791. Assigned to Ametek Corp., 1988.

Selected projects and research positions

Senior Project Leader for the Low-Power VLSI ACMOS Group. Supervise and carry out basic and applied research into CMOS VLSI architectures for applications in low-power and high-performance computing. Recent research investigations have been into decoupled architectures for data-intensive applications and into using high-performance architecture techniques to reduce power dissipation. Previous research pioneered a fundamentally new approach to low-power computing based on the idea of recycling circuit energies in CMOS. Starting with the original idea for "adiabatic charging" in CMOS, led the group into developing the necessary theory to understand the practical trade-offs and taking the most promising approaches forward into VLSI prototypes. The most notable accomplishment was the design, implementation, and demonstration of a 16-bit "clock-powered" microprocessor which used its clock rails as a source of AC power for the on-chip capacitive loads. This three-year long chip development project resulted in a commercial version (MicroDisplay) and our current work in digital signal processing for hearing aids (National Institute of Health) and cellular telephones (Samsung). Most important development in this research endeavor was the invention and subsequent

patenting of the resonant power-clock generation circuitry, which has enabled all of the experiments that were conducted in clock-powered logic.

Technical responsibilities have included mathematical modeling of the circuits and systems, circuit design, VLSI design and layout, compiler development, the design and construction of test fixtures, measurement and characterization of experimental chips, and writing technical papers for scientific publications, including a book chapter in the subject area. Project management responsibilities include supervising full-time research scientists and engineers, and USC graduate students, proposal writing, project planning, budgeting, and progress reporting to government sponsors via written reports and oral presentations.

Architect for a physically-compact, high-performance parallel computer. Developed a packaging-driven architecture based on my earlier research in MCM packaging for modular, parallel computers. The target implementation could execute up to 1.6 gigaflops in a 27 cubic inch, liquid-cooled SEM-E module. Also did the logic design for a message-passing protocol engine that was compatible with the Intel Paragon multicomputer.

Research scientist at the Northrop Research and Technology Center. Developed the conceptual foundations and prototypes for new computer architectures using advanced packaging, interconnection networks, and low-power circuitry. Designed and constructed a one-dimensional self-timed message-passing router chip for application in an MCM-based multicomputer. Northrop patented the input control for asynchronous handshake protocol conversion.

Assistant Professor in Computer Science at the University of Texas at Austin. Working under a small grant from Ametek Corp., carried out research into scalable VLSI architecture concurrent computation. This work consisted of developing concurrent programming systems and large-scale applications for multicomputers. Responsibilities included lecturing in computer architecture and VLSI, and advising graduate and undergraduate students. For an experimental undergraduate VLSI design, developed a simple, 16-bit RISC microprocessor. Served as advisor for two Ph.D. graduate students in their thesis projects. One developed a message-passing cache mechanism to exploit the on-chip cache of a VLSI microprocessor. The other researched instruction-processing resource optimizations for VLSI microprocessors which included research into energy-efficient instruction set design.

Engineering Consultant to Symult Systems Corporation. Hardware and software consultant for the design of the Symult Systems s2010 commercial multicomputer. Principal architect for the node-board computer. Performed complete design and hardware debugging of the node-board's message-handling coprocessor that interfaced to the self-timed (asynchronous) backplane. Defined the synchronization protocol and memory data structures for moving data between the self-timed mesh and the synchronous microprocessor. The design was completed, productized, and commercially offered. Co-inventor of the patented special hardware for the node-board's memory system.

Research Fellow in Computer Science at the California Institute of Technology. Furthered my Ph.D. research studies into VLSI architectures for fine-grain concurrent computation. Investigated new hardware and software mechanisms for executing fine-grain concurrent computations across large networks of small, distributed memory computers.Developed an architecture for a VLSI chip to perform direct memory-to-memory copying of "list" data structures through a message-passing network. Completed the design of a custom chip working with a group of five students. Developed a new instruction set for the Caltech Mosaic

microprocessor and then wrote the microcode that went into the programmed logic arrays of the chip's microcontroller.

Publications

W. Athas, N. Tzartzanis, W. Mao, R. Lal, K. Chong, L. Peterson, M. Bolotski, "Clock-Powered CMOS VLSI Graphics Processor for Embedded Display Controller Application," *2000 IEEE Int'l Solid-State Circuits Conference.*

N. Tzartzanis, W. Athas, "Clock-Powered CMOS: A Hybrid Adiabatic Logic Style for Power-Efficient Computing," *20th Anniversary Conference on Advanced Research in VLSI*, IEEE Computer Society Press, Mar. 1999.

W. Athas, "Low-Power VLSI Techniques for Applications in Embedded Computing," *IEEE Alessandro Volta Memorial Workshop on Low-Power Design*, IEEE Computer Society Press, Mar. 1999.

W. Athas, N. Tzartzanis, L. Svensson, L. Peterson, "A Low-Power Microprocessor Based on Resonant Energy," *IEEE Journal of Solid-State Circuits*, Nov. 1997.

W. Athas, N. Tzartzanis, L. Svensson, L. Peterson, H. Li, X. Jiang, P. Wang, "AC-1: A Clock-Powered Microprocessor," *IEEE Intl. Symposium on Low-Power Electronics and Design*, Aug. 1997.

N. Tzartzanis, W. Athas, "Clock-powered logic for a 50MHz low-power RISC datapath," *1997 IEEE International Solid-State Circuits Conference*, Feb. 1997.

N. Tzartzanis, W. Athas, "Energy recovery for the design of high-speed, low-power static RAMS," *Intl. Symposium on Low-Power Electronics and Design*, Aug. 1996.

W-C Liu, W. Athas, L. Svensson, "Energy-recovery CMOS for highly pipelined DSP designs,". *Intl. Symposium on Low-Power Electronics and Design*, Aug. 1996.

L. Svensson, W. Athas, R. Wen, "A sub-CV^2 pad driver with 10 ns transition time," *Intl. Symposium on Low-Power Electronics and Design*, Aug. 1996.

W. Athas, L. Svensson, N. Tzartzanis, "A resonant signal driver for two-phase, almost-non-overlapping clocks," *Intl. Symposium on Circuits and Systems*, May 1996.

W. Athas, "Energy-Recovery CMOS," in J. Rabaey, M. Pedram (Eds.) *Low-Power Design Methodologies*, Kluwer Academic Press, 1996.

N. Tzartzanis, W. Athas, "Design and analysis of a low-power energy-recovery adder," *Proc. of the Fifth Great Lakes Symposium on VLSI Design*, IEEE Press., Mar. 1995.

W. Athas, N. Tzartzanis, ""Energy Recovery for Low-Power CMOS," *1995 Conference On Advanced Research in VLSI*, Mar. 1995.

W. Athas, L. Svensson, J. Koller, N. Tzartzanis, E. Chou. "Low-power digital systems based on adiabatic-switching principles," *IEEE Transactions on VLSI Systems*, Dec. 1994.

W. Athas, L. Svensson. "Reversible logic issues in adiabatic computing," *Workshop on Physics and Computation*, PhysComp `94, Nov. 1994.

W. Athas, J. Koller. "The architecture and programming of the ISI Embeddable-Variant multicomputer," *1994 Scalable High Performance Computing Conference*, May 1994.

W. Athas, L. Svensson, J. Koller, N. Tzartzanis, Y-C Chou. "A framework for practical low-

EXHIBIT 1
PAGE 11

power digital CMOS systems using adiabatic switching principles," *Int'l Workshop on Low-Power Design.*, Apr. 1994.

W. Athas, J. Koller, L. Svensson. "An energy-efficient CMOS line driver using adiabatic switching," *Proc. of the Fourth Great Lakes Symp. on VLSI Design*, IEEE Press., Mar. 1994

J. Koller, W. Athas "Adiabatic Switching, Low Energy Computing, and the Physics of Storing and Erasing Information," *Proceedings of the Physics of Computation Workshop*, Oct. 1992.

W. Athas. "A Microprocessor Project for an introductory VLSI design class," *Proceedings of 1990 VLSI Education Conference and Exposition*, July 1990.

W. Athas. "Physically-compact, high-performance multicomputers," *Sixth MIT Conference on Advanced Research in VLSI*, Apr. 1990.

W. Athas, C.L. Seitz. "Multicomputers: message-passing concurrent computers," *IEEE Computer*, Aug. 1988.

Research Advising

John Bunda (co-advisor) Thesis title: Instruction-Processing Optimization Techniques for VLSI Microprocessors. Univ. of Texas at Austin. 1993.

Nestoras Tzartzanis (co-advisor) Thesis title: Energy-Recovery Techniques for CMOS Microprocessor Design, Univ. of Southern California. *Expected to graduate in 1997.*

Bengt-Arne Molin, "Opponent" for Ph.D. dissertation, Univ. of Lund, Sweden, 1993.

Courses Taught

- Fall 1998 - VLSI design, graduate level, Univ. of Southern California
- Spring 1998 - VLSI design, graduate level, Univ. of Southern California
- Fall 1997 - VLSI design, graduate level, Univ. of Southern California
- Spring 1995 - VLSI design, graduate level, Univ. of Southern California
- Fall 1994 - VLSI design, graduate level, Univ. of Southern California
- Fall 1992 - Computer architecture, undergraduate level, Univ. of Calif, Irvine.
- Spring 1992 - VLSI design, undergraduate level, Univ. of Calif., Irvine.
- Winter 1992 - Computer architecture, undergraduate level, Univ. of Calif., Irvine.
- Fall 1991 - VLSI design, undergraduate level, Univ. of Texas at Austin.
- Spring 1991 - VLSI design, graduate level, Univ. of Texas at Austin.
- Fall 1990 - Computer architecture, undergraduate level, Univ. of Texas at Austin.

Research interests

- Low-power VLSI circuit design and architectures
- High-speed VLSI circuit design and architectures
- Decoupled architectures for high-performance and low-cost implementations
- VLSI microarchitectures
- Digital signal processing for audio and video

EXHIBIT 1
PAGE 12

- Digital CMOS VLSI circuit design techniques
- Asynchronous and self-timed circuit design
- Reversible computing
- Computational models for parallel and concurrent systems
- Algorithms for device- and switch-level circuit simulation
- Reconfigurable computing ASIC design and implementation
- MCM system design and implementation
- Compiler design and implementation
- Parallel and concurrent programming
- Embedded systems design

Professional activities

Member of the IEEE.

Program committee member, Int'l Solid-States Circuit Conference, 1999-2000.

Program committee member for the International Symposium on Low-Power Electronics and Design, 1998-2000.

Invited speaker at the IEEE Volta Memorial Workshop on Low-Power Design, 1999.

Invited speaker at ESSCIRC 1997.

Expert external assessor for Hong Kong Research Grants Council, University Grants Committee, 1995-1997.

Cited for outstanding paper review by IEEE Computer, 1996.

Program committee member for the International Symposium on Low-Power Electronics and Design, 1995.

Program committee member for the Scalable High-Performance Computing Conference, 1990.

Judge for Los Angeles County Science Fair, Physics & Astronomy, 1995-1997.